

Abstract of the Disclosure

Very complex (multilevel) logical expressions are represented in a vector format. The logic is simplified by identifying opposing couples (a literal and its negation) and replacing symmetrical logic expressions attached to the opposing couples with a single version. Significant simplification of the logic can thus be achieved that is suitable for applications in CAD/CAM and in design and manufacture of integrated circuits. The simplification results in increased reliability, lower cost and faster circuits.